120

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

5/3/04

AF $

2124

PATENT APPLICATION

ATTORNEY DOCKET NO. 10003151-1

OIPE JC13
APR 30 2004
PATENT & TRADEMARK OFFICE

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Joe D. Bolding et al.

Confirmation No.: 3782

Application No.: 09/740,601

Examiner: Trenton J. Roche

Filing Date: Dec. 19, 2000

Group Art Unit: 2124

Title: AUTOMATIC SYMBOL TABLE SELECTION IN A MULTI-CELL ENVIRONMENT

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

RECEIVED
MAY 0 7 2004
Technology Center 2100

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith in **triplicate** is the Appeal Brief in this application with respect to the Notice of Appeal filed on **March 1, 2004**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $330.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( ) one month	$110.00
( ) two months	$420.00
( ) three months	$950.00
( ) four months	$1480.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$330.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

Express Mail Label No. EL969919013US

(X) I hereby certify that this correspondence is being deposited with the United States Postal Service as express mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit: **April 30, 2004**

OR

( ) I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number_____ on _____

Number of pages:

Typed Name: **Kalyn Black**

Signature: Kalyn Black

Respectfully submitted,

Joe D. Bolding et al.

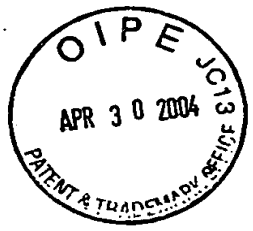
By G K Clinger

Guy K. Clinger, Esq.

Attorney/Agent for Applicant(s)
Reg. No. **42,422**

Date: **April 30, 2004**

Telephone No.: **(303) 298-9888**



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT
APPEALS AND INTERFERENCES

In Re Application of :	)	
	)	
BOLDING, Joe D. et al.	)	
	)	
Serial No.: 09/740,601	)	Group Art Unit: 2124
	)	
Filed: December 19, 2000	)	Examiner: ROCHE, Trenton J.
	)	
For: AUTOMATIC SYMBOL TABLE SELECTION IN A MULTI-CELL ENVIRONMENT	)	Atty Dkt. 10003151-1

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief is submitted in response to the final rejection of the claims mailed January 29, 2004. A Notice of Appeal was filed on March 1, 2004.

(1) REAL PARTY IN INTEREST

The real party in interest in the above-referenced patent application is Hewlett-Packard Development Company, LP, a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

(2) RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences currently known to appellants, appellants' legal representatives or the assignee, which will directly affect, or be directly affected by, or have a bearing on, the Board's decision.

(3) STATUS OF CLAIMS

Claims 1-25 were originally filed with the application, with claims 1-4, 8, 16-19 and 21 being amended in the response filed on December 9, 2003. Claims 1-25 stand rejected in the final Office action mailed January 29, 2004. The rejection of claims 1-25 is appealed.

(4) STATUS OF AMENDMENTS

No amendments were filed or entered subsequent to the final Office action mailed January 29, 2004.

(5) SUMMARY OF THE INVENTION

This invention relates generally to selecting a symbol table, and more specifically to using an address pointer or program counter to select at least one of a plurality of symbol tables (page 6, line 30 - page 7, line 4, claims 1 and 16). A symbol table is a lookup table correlating lines of high level program code, variables, functions, etc with their addresses in a computer memory. (Page 2, lines 29-32)

Multiple symbol tables may be provided when debugging a software program for a computer system having multiple processor cells, each cell having its own memory space. (Page 3, lines 18-24) As the program is assigned to a processor cell and placed in the memory for that cell, the addresses in the symbol table must be adjusted accordingly. (Page 3, lines 24-32) Typically, this has been done by manually calculating an address offset and instructing the debugging tools to add the address offset to the addresses in the symbol table. (Page 3, lines 7-11)

The invention involves providing a plurality of symbol tables, each encompassing a range of addresses. (Page 10, lines 29-32, Claim 1) The addresses in the symbol tables are offset for use when the program is relocated in memory (Page 10, line 32 - Page 11, line 1), such as when

used in a computer system with multiple processing cells wherein the memory locations are known in advance. (Page 11, line 31 - page 12, line 19) The appropriate symbol table is selected by examining the contents of the address pointer or program counter and identifying at least one symbol table whose address range includes the address pointed to by the address pointer or program counter. (Page 11, lines 6-10, claims 1 and 16).

(6) ISSUES

A. Whether claim 1 is unpatentable under 35 U.S.C. §102(b) as being anticipated by Miyadera et al., U.S. Patent 4,769,770 (hereinafter Miyadera).

B. Whether claim 16 is unpatentable under 35 U.S.C. §103(a) over Miyadera in view of Sites, U.S. Patent 5,652,889.

C. Whether claim 23 is unpatentable under 35 U.S.C. 103(a) as being unpatentable over Miyadera in view of On et al., U.S. Patent 6,275,956 (hereinafter On).

D. Whether claim 25 is unpatentable under 35 U.S.C. 103(a) as being unpatentable over Miyadera in view of Canady et al., U.S. Patent 5,742,828 (hereinafter Canady).

(7) GROUPING OF CLAIMS

Dependent claims 2-15 stand or fall with independent claim 1. Dependent claims 17-22 stand or fall with independent claim 16. Dependent claim 24 stands or falls with independent claim 23. None of the other claims stand or fall together. Claims 1, 16, 23 and 25 have not been grouped together because of the different reasons for allowability presented below for each.

(8) ARGUMENT

Relevant Law

Legal Basis for Anticipation Under 35 U.S.C. §102 and for Obviousness Under 35 U.S.C. §103

The standard for lack of novelty, that is, for "anticipation," under 35 U.S.C. §102 is one of strict identity. To anticipate a claim for a patent, a single prior source must contain all its essential elements. Hybritech, Inc. v. Monoclonal Antibodies, Inc., 231 USPQ 81, 90 (Fed. Cir. 1986). Invalidity for anticipation requires that all of the elements and limitations of the claims be found within a single prior art reference. Scripps Clinic & Research Foundation v. Genentech, Inc., 18 USPQ2d 1001 (Fed. Cir. 1991).

The test for obviousness under 35 U.S.C. 103 is whether the claimed invention would have been obvious to those skilled in the art in

light of the knowledge made available by the reference or references. *In re Donovan*, 184 USPQ 414, 420, n. 3 (CCPA 1975). It requires consideration of the entirety of the disclosures of the references. *In re Rinehart*, 189 USPQ 143, 146 (CCPA 1976). All limitations of the Claims must be considered. *In re Boe*, 184 USPQ 38, 40 (CCPA 1974). In making a determination as to obviousness, the references must be read without benefit of applicants' teachings. *In re Meng*, 181 USPQ 94, 97 (CCPA 1974). In addition, the propriety of a Section 103 rejection is to be determined by whether the reference teachings appear to be sufficient for one of ordinary skill in the relevant art having the references before him to make the proposed substitution, combination, or other modifications. *In re Lintner*, 173 USPQ 560, 562 (CCPA 1972).

In the case of *In re Wright*, 6 USPQ 2d 1959 (CAFC 1988), the CAFC decided that the Patent Office had improperly combined references which did not suggest the properties and results of the applicants' invention nor suggest the claimed combination as a solution to the problem which applicants' invention solved.

The CCPA reached this conclusion after an analysis of the prior case law, at p. 1961:

> We repeat the mandate of 35 U.S.C. 103: it is the invention as a whole that must be considered in obviousness determinations. The invention as a whole embraces the structure, its properties, and the problem it solves. See, e.g., *Cable Electric Products, Inc. v. Genmark, Inc.*, 770 F.2d 1015, 1025, 226 USPQ 881, 886 (Fed. Cir. 1985) ("In evaluating obviousness, the hypothetical person of ordinary

skill in the pertinent art is presumed to have the 'ability to select and utilize knowledge from other arts reasonably pertinent to [the] particular problem' to which the invention is directed"), quoting *In re Antle*, 444 F.2d 1168, 1171-72, 170 USPQ 285, 287-88 (CCPA 1971); *In re Antonie*, 559 F.2d 618, 619, 195 USPQ 6, 8 (CCPA 1977) ("In delineating the invention as a whole, we look not only in the claim in question... but also to those properties of the subject matter which are inherent in the subject matter and are disclosed in the specification") (emphasis in original).

The determination of whether a novel structure is or is not "obvious" requires cognizance of the properties of that structure and the problem which it solves, viewed in light of the teachings of the prior art. See, e.g., *In re Rinehart*, 531 F.2d 1048, 1054, 189 USPQ 143, 149 (CCPA 1976) (the particular problem facing the inventor must be considered in determining obviousness); see also *Lindemann Maschinenfabrik GmbH v. American Hoist and Derrick Co.*, 730 F.2d 1452, 1462, 221 USPQ 481, 488 (Fed. Cir. 1984) (it is error to focus "solely on the product created, rather than on the obviousness or notoriousness of its creation") (quoting *General Motors Corp. v. U.S. Int'l Trade Comm'n*, 687 F.2d 476, 483, 215 USPQ 484, 489 (CCPA 1982), cert. denied, 459 U.S. 1105 (1983).

Thus the question is whether what the inventor did would have been obvious to one of ordinary skill in the art attempting to solve the problem upon which the inventor was working. *Rinehart*, 531 F.2d at 1054, 189 USPQ at 149; see also *In re Benno*, 768 F.2d 1340, 1345, 226 USPQ 683, 687 (Fed. Cir. 1985) ("appellant's problem" and the prior art present different problems requiring different solutions").

A basic mandate inherent in Section 103 is that a piecemeal reconstruction of prior art patents shall not be the basis for a holding of

obviousness. It is impermissible within the framework of Section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. *In re Kamm*, 172 USPQ 298, 301-302 (CCPA 1972). Phrased somewhat differently, the fact that inventions of the references and of applicants may be directed to concepts for solving the same problem does not serve as a basis for arbitrarily choosing elements from references to attempt to fashion applicants' claimed invention. *In re Donovan*, 184 USPQ 414, 420 (CCPA 1975).

It is also clearly established in the case law that a change in the mode of operation of a device which renders that device inoperative for its stated utility as set forth in the cited reference renders the reference improper for use to support an obviousness-type rejection predicated on such a change. See, e.g., *Diamond International Corp. v. Walterhoefer*, 289 F.Supp. 550, 159 USPQ 452, 460-61 (D.Md. 1968); *Ex parte Weber*, 154 USPQ 491, 492 (Bd.App. 1967). In addition, any attempt to combine the teaching of one reference with that of another in such a manner as to render the invention of the first reference inoperative is not permissible. See, e.g., *Ex parte Hartmann*, 186 USPQ 366 (Bd.App. 1974); and *Ex parte Sternau*, 155 USPQ 733 (Bd.App. 1967).

A reference which teaches away from the applicants' invention may not properly be used in framing a 35 U.S.C. 103 rejection of

applicants' claims. See *United States v. Adams*, 148 USPQ 429 (Sup. Ct. 1966).

Argument re Issue A

Claim 1 stands rejected under 35 U.S.C. §102(b) as being anticipated by Miyadera, U.S. Patent 4,769,770.

It is submitted that claim 1 is not unpatentable over Miyadera, and that, further, the invention recited by claim 1 is not disclosed or suggested by any of the prior art of record, considered either alone or in proper combination.

Claim 1

Appellants' claim 1 recites the following:

A method of selecting a symbol table, comprising:

providing a plurality of symbol tables in a computer system, said computer system having an address pointer, each of said symbol tables encompassing a range of addresses; and

selecting at least one of said plurality of symbol tables within whose range of addresses said address pointer is pointing.

Claim 1 recites the following:

providing a plurality of symbol tables and

selecting at least one of said plurality of symbol tables

The Examiner takes the position that Miyadera discloses this recitation, referring to Miyadera, col. 6, line 39, which states that "**a plurality of relocation tables may be provided.**"

Appellants respectfully disagree with the Examiner's position. The disclosure of Miyadera is not directed at the selection of a symbol table, but at the relocation of a logical address to form a real address. Although Miyadera does disclose a table (relocation table), this is **not** a symbol table. Miyadera does not disclose a method of selecting a symbol table, but a method of altering a portion of a logical address to form a real address using a relocation table. (See Miyadera, col. 1, line 1 - col. 2, line 5, col. 2, lines 43-57) Miyadera does disclose providing a plurality of relocation tables, and their selection using a pointer, as follows:

> " In order to reduce an overhead during changing the space, a plurality of relocation tables may be provided. In this case, the content corresponding to each job is written in each of the relocation tables, and pointers are provided for identifying the relocation tables. Thus, the relocation tables are selected in a software fashion by using the content of the pointer." (Miyadera, col. 6, lines 37-44)

However, these tables are relocation tables, not symbol tables. The Examiner has cited the definition of a symbol table from the IEEE

Standard Dictionary of Electrical and Electronics Terms, Sixth Edition, IEEE Std 100-1996, as follows:

"A table that presents program symbols and their corresponding addresses, values, and other attributes."

Appellants respectfully believe that this definition of a symbol table in fact points out the difference between Miyadera's relocation tables and the symbol tables of Appellants' claim 1. Miyadera's relocation table does not present **program symbols *and*** their corresponding addresses, but simply a list of partial logical addresses used to form real addresses, as described in Miyadera, col. 3, lines 39-48:

> "In address relocation, the logical address is divided into the upper and lower portions. If the upper address is present within a predetermined address range to be relocated, the relocation table is looked up by a predetermined address portion of the upper address to read an entry. The real address is obtained by adding the entry and the lower address. With the address relocation, the address range capable of being identified by the lower address is simply relocated by changing the upper address."

The process of using a relocation table to form a real address is described in more detail in Miyadera, col. 5, line 53 - col. 6, line 11, and clearly does not present **program symbols and their corresponding addresses** in a relocation table. Clearly, Miyadera fails to disclose or suggest providing or selecting a **plurality of symbol tables**. To

anticipate a claim for a patent, a single prior source must contain all its essential elements. Hybritech, Inc. v. Monoclonal Antibodies, Inc., 231 USPQ 81, 90 (Fed. Cir. 1986). Invalidity for anticipation requires that all of the elements and limitations of the claims be found within a single prior art reference. Scripps Clinic & Research Foundation v. Genentech, Inc., 18 USPQ2d 1001 (Fed. Cir. 1991).

Argument re Issue B

Claim 16 stands rejected under 35 U.S.C. §103(a) over Miyadera in view of Sites, U.S. Patent 5,652,889.

It is submitted that claim 16 is not unpatentable over Miyadera and Sites, and that, further, the invention recited by claim 16 is not disclosed or suggested by any of the prior art of record, considered either alone or in proper combination.

Claim 16

Appellants' claim 16 recites the following:

An apparatus for automatically selecting a symbol table in a computer having a program counter and a plurality of symbol tables, the apparatus comprising:

a) at least one computer readable storage medium; and

b) computer readable program code stored on the at least one computer readable storage medium, the computer readable program code comprising code for selecting one of said plurality of symbol tables wherein said program counter in said computer contains an address within said one of said plurality of symbol tables.

Miyadera does not disclose or suggest providing or selecting a plurality of symbol tables as discussed above with respect to claim 1, and furthermore, Sites does nothing to remedy this inadequacy. Sites does not disclose or suggest multiple symbol tables. Sites is cited as disclosing a program counter "in an analogous memory address relocation system" to that of Miyadera. Appellants respectfully disagree that Sites discloses a memory address relocation system analogous to that of Miyadera, but even assuming for the sake of argument that they are analogous, neither is directed to the selection of one of a plurality of symbol tables. Whereas Miyadera was directed to converting logical addresses to real addresses in a multiprocessor system, Sites is directed at alternately executing translated portions of a computer program and interpreting original portions of the computer program (see Sites, Abstract). Sites does not address the problem of selecting one of a plurality of symbol tables. In particular, Sites does not disclose the use of the program counter for selecting one of a plurality of any type of table, wherein the program counter contains an address within one of the tables.

For example, the Examiner has referred to Sites, col. 10, line 55, which states that "if the program counter is addressed, the value of the program counter itself is incremented which causes program execution to jump over operand data or an operand address disposed in the instruction stream." Clearly this does not disclose that the program counter contains an address within one of a plurality of tables to be selected, let alone one

of a plurality of symbol tables. Each reference in Sites to the program counter is directed to some aspect of software translation, such as generating histograms (see Sites, col. 13, lines 61-65), or to offsetting the program counter to jump between program blocks (see Sites, col. 34, lines 46-55), etc. Sites does not disclose or suggest the use of a program counter to select one of a plurality of tables, symbol or otherwise. Because even the proposed combination of references fails to disclose or suggest all of the limitations of claim 16, the Examiner has failed to establish a *prima facie* case of obviousness with respect to claim 16.

Appellants further respectfully assert that a *prima facie* case of obviousness has not been established because there is no teaching or suggestion to combine the Miyadera and Sites references as proposed by the Examiner. "It is insufficient to establish obviousness that the separate elements of the invention existed in the prior art, absent some teaching or suggestion, in the prior art, to combine the elements." *Arkie Lures, Inc. v. Gene Larew Tackle, Inc.*, 119 F.3d 953, 957, 43 USPQ2d 1294, 1297 (Fed. Cir. 1997). The piecemeal selection of a plurality of relocation tables from Miyadera and a program counter from Sites is not a proper basis for an obviousness rejection under 35 U.S.C. §103. A basic mandate inherent in Section 103 is that a piecemeal reconstruction of prior art patents shall not be the basis for a holding of obviousness. It is impermissible within the framework of Section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation

of what such reference fairly suggests to one of ordinary skill in the art. *In re Kamm*, 172 USPQ 298, 301-302 (CCPA 1972).

Argument re Issue C

Claim 23 stands rejected as being unpatentable under 35 U.S.C. 103(a) over Miyadera in view of On et al., U.S. Patent 6,275,956 (hereinafter On).

It is submitted that claim 23 is not unpatentable over Miyadera and On, and that, further, the invention recited by claim 23 is not disclosed or suggested by any of the prior art of record, considered either alone or in proper combination.

Claim 23

Appellants' claim 23 recites the following:

A debugging apparatus, comprising:

a computer having a plurality of symbol tables stored thereon;

a debugger connected to said computer; and

automatic symbol table selection means for automatically selecting at least one of said plurality of symbol tables in said computer for said debugger.

Miyadera does not disclose or suggest a computer having a plurality of symbol tables stored thereon, nor means for automatically

selecting at least one of the symbol tables, as discussed above with respect to claim 1, and furthermore, On does nothing to remedy this inadequacy. Although On does disclose a parallel debugging apparatus (see Abstract) for use with a cluster parallel computer (col. 3, line 53), On discloses only a single symbol table, not multiple tables, and therefore does not disclose or suggest any method of selecting among a plurality of symbol tables. Therefore, a combination of an address relocation system from Miyadera, even one having multiple relocation tables, with a parallel debugging apparatus having a single symbol table from On would not disclose or suggest all of the limitations of claim 23. On fails to remedy the inadequacies of Miyadera. Because the proposed combination of references fails to disclose or suggest all of the limitations of claim 23, the Examiner has failed to establish a *prima facie* case of obviousness with respect to claim 23.

Appellants further respectfully assert that the Examiner has failed to establish a *prima facie* case of obviousness because there is no teaching or suggestion to combine the Miyadera and On references as proposed by the Examiner. "It is insufficient to establish obviousness that the separate elements of the invention existed in the prior art, absent some teaching or suggestion, in the prior art, to combine the elements." *Arkie Lures, Inc. v. Gene Larew Tackle, Inc.*, 119 F.3d 953, 957, 43 USPQ2d 1294, 1297 (Fed. Cir. 1997).

Argument re Issue D

Claim 25 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Miyadera in view of Canady et al., U.S. Patent 5,742,828 (hereinafter Canady).

It is submitted that claim 25 is not unpatentable over Miyadera and Canady, and that, further, the invention recited by claim 25 is not disclosed or suggested by any of the prior art of record, considered either alone or in proper combination.

Claim 25

Appellants' claim 25 recites the following:

An apparatus for automatically selecting a symbol table in a computer having a plurality of processing cells and having a plurality of symbol tables stored thereon, each of said plurality of symbol tables having a cell identification to indicate for which of said plurality of processing cells it is intended, the apparatus comprising:

a) at least one computer readable storage medium; and

b) computer readable program code stored on said at least one computer readable storage medium, the computer readable program code comprising code for selecting at least one

symbol table which is intended for use with the processing cell which is executing said computer readable program code.

Miyadera does not disclose or suggest a computer having a plurality of symbol tables with cell identifications stored thereon, nor program code for selecting a symbol table intended for use with a cell executing the code. Furthermore, Canady does nothing to remedy this inadequacy. Canady is cited as disclosing "symbol tables having a cell identification."

Appellants respectfully disagree. It is noted that Canady does not disclose a multi-celled computing environment as in claim 25. Furthermore, although Canady does disclose multiple symbol tables, this is to separate global identifiers and local identifiers, and there is no disclosure or suggestion that the multiple symbol tables contain cell identifications:

> "In the preferred embodiment of the invention, separate symbol tables are generated for identifiers available globally (referred to herein as a global symbol table), and for identifiers available within each object declared in the source code 10. Separate symbol tables associated with the application library and with each application object it defines also are generated in the preferred embodiment."
> (Canady, lines 56-63)

Canady does not appear to disclose any method of selecting an appropriate symbol table, but rather, searches **all** symbol tables

"associated with the application libraries made available to it...". (Col. 6, lines 57-58) The identifier referred to in the rejection, discussed at col. 6, line 41 of Canady, is not a cell identifier, but appears to be a possible symbol. The cited portion of Canady is directed to determining whether a portion of the source code is a symbol in any symbol table, rather than selecting an appropriate symbol table based on a cell identification in the symbol table. (See Canady, col. 6, lines 15-23, col. 6, lines 40-46) Miyadera and Canady, therefore, considered either alone or in proper combination, do not disclose or suggest each and every element of claim 25. Miyadera does not disclose multiple symbol tables. Canady does disclose multiple symbol tables, but discloses that all symbol tables are searched for a symbol. Neither discloses cell identifiers in a symbol table.

Appellants note that the Canady contains multiple symbol tables because global and local symbols are separated in different symbol tables. In contrast, Appellants' multiple symbol tables of claim 25 are destined for execution by various processing cells in a computer and contain cell identifiers indicating for which processing cell they are intended. Canady contains no such disclosure. Therefore, Canady fails to remedy the inadequacies of Miyadera. Because the proposed combination of references fails to disclose or suggest all of the limitations of claim 25, the Examiner has failed to establish a *prima facie* case of obviousness with respect to claim 25.

Appellants further respectfully assert that the Examiner has failed to establish a *prima facie* case of obviousness because there is no teaching or suggestion to combine the Miyadera and Canady references as proposed by the Examiner. "It is insufficient to establish obviousness that the separate elements of the invention existed in the prior art, absent some teaching or suggestion, in the prior art, to combine the elements." *Arkie Lures, Inc. v. Gene Larew Tackle, Inc.*, 119 F.3d 953, 957, 43 USPQ2d 1294, 1297 (Fed. Cir. 1997). The motivation proposed by the Examiner to combine Canady with Miyadera is that the "cell identification properties of Canady et al in the address relocation system of Miyadera et al ... would ensure that only one processor is attempting to relocate objects at any one time in the system disclosed by Miyadera et al." Appellants respectfully disagree with this for several reasons. First, as discussed above, Canady does not disclose a cell identifier in each of a plurality of symbol tables, identifying for which cell each symbol table is intended. Furthermore, it is unclear how adding cell identification properties to a plurality of symbol tables would ensure that only one processor relocates objects at any one time, or why this would even be a problem. Miyadera discloses no problem with multiple processors simultaneously attempting to relocate objects. The simple, conventional address relocation system disclosed by Miyadera for forming real addresses from logical addresses would presumably convert one address at a time in each processor as the addresses pass through the processor pipelines, and cell identification in symbol tables has nothing to do with

this address relocation system. Finally, Appellants have not disclosed any need to "ensure that only one processor is attempting to relocate objects at any one time." As disclosed in Appellants' Background, a software program is moved into the memory space for one of a plurality of processors in a multi-processor computer, and the corresponding symbol table for that memory space is selected for use by a debugger. This does not indicate that a problem exists with multiple processors simultaneously attempting to relocate objects. Therefore, Appellants' respectfully disagree that any motivation exists to combine Canady with Miyadera as proposed by the Examiner. "It is insufficient to establish obviousness that the separate elements of the invention existed in the prior art, absent some teaching or suggestion, in the prior art, to combine the elements." *Arkie Lures, Inc. v. Gene Larew Tackle, Inc.*, 119 F.3d 953, 957, 43 USPQ2d 1294, 1297 (Fed. Cir. 1997). Furthermore, because even the Examiner's proposed (improper, as discussed above) combination of references fails to teach all of the limitations of claim 25, a *prima facie* case of obviousness has not been established.

Accordingly, all of the claims are believed to be allowable and all of the rejections should be reversed.

Respectfully submitted,

KLAAS, LAW, O'MEARA & MALKIN, P.C.

By _____

Guy K. Clinger
Registration No. 42,422
1999 Broadway, Suite 2225
Denver, CO 80202
(303) 298-9888

(9) APPENDIX

1. A method of selecting a symbol table, comprising:

providing a plurality of symbol tables in a computer system, said computer system having an address pointer, each of said symbol tables encompassing a range of addresses; and

selecting at least one of said plurality of symbol tables within whose range of addresses said address pointer is pointing.

2. The method of claim 1, wherein a debugger connected to said computer system performs said selecting of said at least one of said plurality of symbol tables.

3. The method of claim 2, wherein said selecting is performed each time said debugger transitions from an executing mode to a command mode.

4. The method of claim 1, wherein said computer system performs said selecting of said at least one of said plurality of symbol tables.

5. The method of claim 1, wherein said address pointer comprises a pointer to a memory location containing instructions to be executed.

6. The method of claim 5, wherein said pointer comprises a program counter.

7. The method of claim 1, wherein said computer system comprises a plurality of cells, each of said cells comprising a processing unit having at least one computer processor, the method further comprising identifying an active cell among said plurality of cells, wherein said symbol table is being selected for said active cell.

8. The method of claim 7, wherein said plurality of symbol tables includes at least one base symbol table and a plurality of secondary symbol tables, and wherein said selecting said at least one of said plurality of symbol tables comprises:

examining said at least one base symbol table to determine whether said address pointer is pointing within said at least one base symbol table; and

examining at least one of said plurality of secondary symbol tables to determine whether said address pointer is pointing within said at least one of said plurality of secondary symbol tables, wherein said at

least one of said plurality of secondary symbol tables is associated with said active cell.

9. The method of claim 8, wherein said plurality of symbol tables are contained in a symbol table set, and wherein each of said plurality of secondary symbol tables comprise a reference to a base symbol table, a cell identifier, and an address offset specifying an offset from said base symbol table.

10. The method of claim 8, wherein said at least one base symbol table is examined before said at least one of said plurality of secondary symbol tables is examined.

11. The method of claim 8, wherein said at least one of said plurality of secondary symbol tables is only examined if said address pointer is not pointing within said at least one base symbol table.

12. The method of claim 8, wherein said examining at least one of said plurality of secondary symbol tables comprises checking a cell identifier within each of said plurality of secondary symbol tables to determine whether each of said plurality of secondary symbol tables is associated with said active cell, and examining only tables within said plurality of secondary symbol tables which are associated with said

active cell to determine whether said tables which are associated with said active cell should be selected.

13. The method of claim 1, wherein said at least one of said plurality of symbol tables is selected by marking said at least one of said plurality of symbol tables as active.

14. The method of claim 13, further comprising a debugger using a symbol table among said plurality of symbol tables which is marked as active.

15. The method of claim 1, wherein said computer system comprises an architectural simulator.

16. An apparatus for automatically selecting a symbol table in a computer having a program counter and a plurality of symbol tables, the apparatus comprising:

a) at least one computer readable storage medium; and

b) computer readable program code stored on the at least one computer readable storage medium, the computer readable program code comprising code for selecting one of said plurality of symbol tables wherein said program counter in said computer contains an address within said one of said plurality of symbol tables.

17. The apparatus of claim 16, wherein each of said plurality of symbol tables includes symbols stored within an address range, and wherein said code for selecting said one of said plurality of symbol tables comprises determining whether said program counter contains an address within said address range for said one of said plurality of symbol tables.

18. The apparatus of claim 16, wherein said code for selecting one of said plurality of symbol tables comprises code for determining whether said program counter contains an address within a base symbol table in said plurality of symbol tables.

19. The apparatus of claim 16, wherein said code for selecting one of said plurality of symbol tables comprises code for determining whether said program counter contains an address within an offset symbol table in said plurality of symbol tables.

20. The apparatus of claim 19, wherein said computer comprises a plurality of processing cells.

21. The apparatus of claim 20, wherein said code for selecting one of said plurality of symbol tables further comprises code for determining whether a cell identifier in said offset symbol table refers to one of said plurality of processing cells which is executing said computer readable program code.

22. The apparatus of claim 16, further comprising code for determining whether said one of said plurality of symbol tables is enabled for automatic selection.

23. A debugging apparatus, comprising:

a computer having a plurality of symbol tables stored thereon;

a debugger connected to said computer; and

automatic symbol table selection means for automatically selecting at least one of said plurality of symbol tables in said computer for said debugger.

24. The debugging apparatus of claim 23, wherein said computer comprises a plurality of processing cells.

25. An apparatus for automatically selecting a symbol table in a computer having a plurality of processing cells and having a plurality of symbol tables stored thereon, each of said plurality of symbol tables having a cell identification to indicate for which of said plurality of processing cells it is intended, the apparatus comprising:

a) at least one computer readable storage medium; and

b) computer readable program code stored on said at least one computer readable storage medium, the computer readable program code comprising code for selecting at least one symbol table which is intended

for use with the processing cell which is executing said computer readable program code.